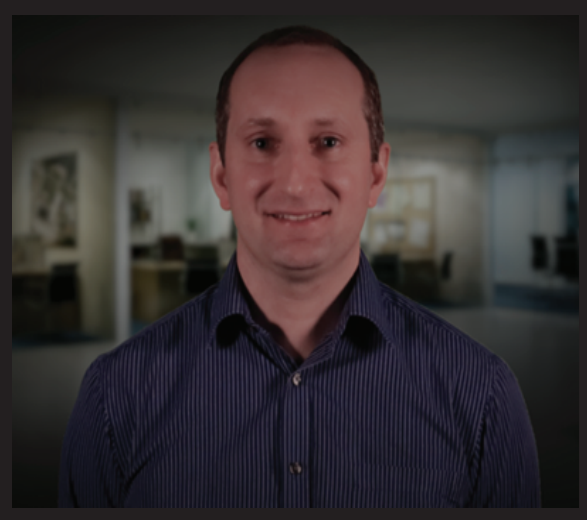
SCHOOL OF COMPUTING
UNIVERSITY OF UTAH

# Distinguished Lecture

2pm - Thurs. April 7, 2022
IN-PERSON: WEB L110

ZOOM option also available:
Mtg. ID: 930 0776 9283
Passcode: TheoDrane



# The Numerical Hardware Design Landscape Challenges and Opportunities


## Dr. Theo Drane
## Intel's Accelerated Computing Systems and Graphics Group



Abstract: Numerical hardware design is most challenging and most valuable when the hardware concerned is dominated by diverse and evolving compute tasks, and pushed to the limit in terms of needing low area, high frequency & low power consumption. GPU hardware design offers such a multi-faceted challenge. This talk will walk through the potency of optimizations at an algorithm, number format, precision, accuracy and logic gate level; show key examples of hardware design space definition and exploration, and the general challenges of doing so: algorithm design, specification creation, modelling, hardware implementation & optimization with formal verification and validation used throughout

While we may hand craft critical numerical hardware kernels, we seek to take such insights, through generalization and ultimately toward automation.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Bio: Dr. Theo Drane started working for the Datapath consultancy, Arithmatica, in 2002 after a Mathematics degree from the University of Cambridge, UK.

He moved to Imagination Technologies in 2005, where he subsequently founded their Datapath team while studying for a PhD at Imperial College London's EE Department.

In December 2018, after a stint within Cadence Design System's Logic Synthesis division, Genus, he joined Intel's Accelerated Computing Systems and Graphics Group.

There, he leads and is building an applied research Numerical Hardware group which focuses on all aspects of architecting, implementing, optimizing and formally verifying math intensive hardware.